Qeios

Peer Review

Review of: "Calibrating DRAMPower Model: A Runtime Perspective from Real-System HPC Measurements"

Khaled Mahmoud[1]

1. State University of New York at Binghamton, United States

Claim and Contribution:

The paper clearly claims to enhance RAM energy estimation by 5% through the calibration of DRAMPower. The objective and problem statement of the research are well stated and clear. The research paper has potential, and I believe the researchers should pursue the publication of their paper and add missing artifacts according to the feedback provided.

Key Feedback:

Methodology Details:

While the claim is compelling, the paper lacks sufficient detail about the calibration methodology. Specifically, it does not explain how the calibration process is conducted or validated against unseen workloads, which raises concerns about its generalizability.

System Configuration:

The paper mentions using a 2-socket Haswell system but does not specify the exact CPU model. Haswell processors, as per Intel's website (Intel Haswell Product Line), come in various configurations, including models with 18, 14, 12, 10, 8, 6, and 4 cores. Based on the results, the system appears to use a 12-core CPU. However, the CPU product number (e.g., E7-8870V3) and full specifications should be included for clarity and reproducibility.

Background Section:

The paper would benefit from a dedicated background section explaining key concepts, such as:

- **Dynamic vs. Static Power:** When RAM transitions to static power.

doi.org/10.32388/5P591H

- **IDD Currents:** For example, IDD5 (refresh current) and other IDD currents relevant to the study should be defined and explained. These concepts should either be introduced in the introduction or expanded in a background section.

Energy Equation:

The provided energy equation,

1. $E_{cmd} = V_{dd} \times T_{op} \times N_{bank} \times I_{op} \times N_{cmd}$

requires more elaboration. It does not clearly represent how IDD currents contribute to energy consumption for specific commands. A detailed breakdown of how each current is factored in is necessary.

Analysis of Results (Figure 2):

Figure 2 shows the power relationship with the number of threads but provides minimal explanation. Observations include:

- DDRAB and DDRCD stabilize and peak at 7 threads, while DDREF and DDRGH steadily increase from 12 to 24 threads.

  More insights and analysis are needed to interpret these patterns meaningfully.

Benchmarks:

The benchmarks used are more akin to microbenchmarks than actual workloads. Calibration appears to be performed exclusively at maximum thread utilization. The absence of diverse and realistic workloads undermines the robustness of the evaluation.

Calibration Details and Validation:

The paper does not provide sufficient details about how DRAMPower is calibrated. Furthermore, it is unclear if these calibration values have been tested and validated on unseen memory workloads. Addressing this gap is crucial for demonstrating the research's generalizability and applicability.

Declarations

Potential competing interests: State University of New York at Binghamton Intel Corporation