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Peer Review

Review of: "Negative Capacitance Effect at the Interface Between Si Wafers with Undulating Surfaces"

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In this manuscript, the authors present a novel structure exhibiting negative capacitance behavior between two silicon wafers. Before considering it further, I have a few suggestions and questions. Please find my comments below:

1. The paper discusses frequency-dependent behavior, but what are the transient response characteristics of the system? Could there be hysteresis effects in capacitance-voltage measurements? Such information would provide additional insights into the stability and usability of this effect in real-world applications.

2. The undulating interface likely induces strong electrostatic fringing fields. Could the authors provide insights into how these fields might locally modify capacitance behavior? A simulation or qualitative discussion would clarify whether these effects contribute significantly to the observed negative capacitance.

3. The authors should discuss potential parasitic capacitances and how they have been mitigated in measurements. Given the small-scale interface and vacuum gaps, factors like stray capacitance and measurement artifacts could influence the results. How were these accounted for experimentally?

4. The discussion preceding Figure 6 would benefit from an equivalent circuit diagram illustrating the interplay between resistance, tunneling current, and capacitance. This will help readers better

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understand the transition between positive and negative capacitance.

5. The paper should explicitly describe the mechanisms leading to negative capacitance at the Si interface. While the role of tunneling current is mentioned, a more quantitative or conceptual discussion about charge accumulation, depletion, and electrostatic effects in the context of existing negative capacitance models would strengthen the argument.

Declarations

Potential competing interests: No potential competing interests to declare.