Qeios

Peer Review

Review of: "WebRISC-V: A 64-bit RISC-V Pipeline Simulator for Computer Architecture Classes"

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This paper tackles a very relevant problem: helping students grasp the details of pipelined execution of RISC-V processors.

The tool does a good job of giving feedback to students and showing the state of the processor. However, I do not see significant differences from the previous articles on the subject by the authors.

I think some aspects could be improved.

* The details of the processor model implementation and the simulation environment used are not described. The paper only mentions that it is based in PHP.

* The authors mention that creating programs with gcc is avoided. Since the pipeline is a kind of complex concept for students to understand, I assume they should be able to understand code compiled by gcc at this level. I understand that providing assembly limits the size of the programs to analyze, but at the same time, it makes them less realistic.

* Pipeline execution sequences should mention the following reference for konata diagrams (provided for Gem5).

Ryota Shioya. 2022. Konata. https://github.com/shioyadan/Konata.

* The described use cases should clearly describe several scenarios affecting the pipeline. It would be nice to clearly show all the potential causes of pipeline bubbles and pipeline flushes, with an explanation that links to the observed diagram. The current description is very limited.

doi.org/10.32388/FD9BH8

Declarations

Potential competing interests: No potential competing interests to declare.