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Peer Review

Review of: "WebRISC-V: A 64-bit RISC-V Pipeline Simulator for Computer Architecture Classes"

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As an instructor in computer architecture, I found the web-based tool presented to be highly effective for teaching fundamental concepts. It offers an intuitive and visually rich representation of the processor pipeline, which greatly enhances student understanding. I found features such as the ability to toggle between the data path, control path, and other components very helpful. Additionally, the option to step through individual clock cycles provides valuable insight into the behavior of the processor.

I personally explored the tool via the GitHub link provided and was impressed with its functionality and ease of use. This is a valuable contribution to the educational resources available to the computer engineering community, and I fully intend to incorporate it into my future courses. Thank you for making such a practical tool available.

That said, the primary concern with the current manuscript is that it does not meet the criteria of a traditional “research” article. While the work is certainly worth publishing, it would be better suited for venues that have a dedicated “educational” or “tools and resources” track.

If you are planning to submit to such venues, I recommend the following improvements:

1. Include references or links to other existing web-based tools to provide context.
2. Present a comparative analysis in tabular form, evaluating key metrics such as performance, ease of access, usability, back-end and front-end platforms, etc.
3. Offer some insight into the educational impact of the tool. You can compare student learning outcomes before and after incorporating the tool. Quantitative and qualitative data from classroom use would significantly strengthen the paper.

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Declarations

Potential competing interests: No potential competing interests to declare.