Research Article

WebRISC-V: A 64-bit RISC-V Pipeline Simulator for Computer Architecture Classes

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WebRISC-V is a web-based educational tool designed to simulate the pipelined execution of assembly programs according to the RV64IM specifications (64-bit RISC-V processor). The tool allows users to investigate pipeline stalls, understand the internal state of pipeline architectural blocks, and visualize the cycle-by-cycle execution of instructions. WebRISC-V executes directly in a web browser, providing a detailed pipeline execution for RISC-V processors. This paper describes the features of WebRISC-V, compares it with similar tools, and provides an example of its usage in investigating the pipeline.

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1. Introduction

Instruction pipelining is a fundamental concept in Computer Architecture courses, as it significantly improves processor performance. However, its real impact is often underestimated or misunderstood by students. WebRISC-V addresses this educational gap by offering an interactive, user-friendly web-based tool for visualizing and analyzing execution.

Understanding pipeline, including stalls and hazards, is crucial in optimizing performance. WebRISC-V provides a cycle-by-cycle analysis of RISC-V instructions in a pipeline, allowing a deeper understanding of execution flow, instruction dependencies, and bottlenecks that affect speedup.

2. Key Features and Contributions

WebRISC-V introduces several innovations that distinguish it from existing tools, including:

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- A browser-based interface requiring no installation, making it accessible from any device.
- Cycle-accurate visualization of pipeline execution, via instruction flow and hazard detection.
- Identification and classification of stalls, hazards, and structural dependencies within the pipeline.
- Interactive features for modifying instructions and observing real-time execution changes.
- A comparison of different execution sequences, providing insights into pipeline optimization.
- Automatic generation of detailed pipeline execution diagrams, aiding in teaching and research.
- A comparison with other available pipeline visualization tools, highlighting WebRISC-V's advantages in usability and accuracy.

3. Other Existing Pipeline Tools

Several tools exist for visualizing pipeline execution, but most require local installation and lack detailed cycle-by-cycle analysis. WebRISC-V stands out due to its web-based accessibility and real-time feedback. Tools such as Ripes and QtSPIM provide some pipeline visualization but do not offer the level of detail or interactivity as WebRISC-V. By allowing users to interact directly with the execution process, WebRISC-V serves as a more effective learning tool. PBSE, (MARS plug-in), MIPS X-Ray (MARS plug-in), DrMIPS, Mipster32, UCOMIPSIM, Visimips, WASP and WebMIPS are MIPS ISA tools; Ripes[1] and WebRISC-V are similar tools, but supporting the RISC-V ISA. While Ripes supports gcc-compiled code and is more tailored to developers, WebRISC-V restricts the supported ISA to 'RV64IM' to provide an environment more focused on educational principles.

3.1. Software Architecture

WebRISC-V has its back-end written in PHP and its front-end in HTML, CSS and JavaScript[2]. Being a server-side web application, it is installed and executed on a web server and presented to the user on their client interface. If the teaching staff wants a local installation, an instance can be hosted with a simple procedure on a Linux or Windows server.

This simulator supports the full implementation of two RISC-V 'modules'[2] as they are described in the RISC-V ISA unprivileged specification[3]: the 64-bit Base Integer ("fence" instruction excluded) module - also called 'RV64I' module - and the Extension for Integer Multiplication and Division module - also called 'M' module, therefore making the tool run according to the 'RV64IM' specification.

Voluntarily, for easier student reference, WebRISC-V closely resembles the schematic used in the Patterson/Hennessy book[4], in which the pipelined datapath implementation is explored and explained.

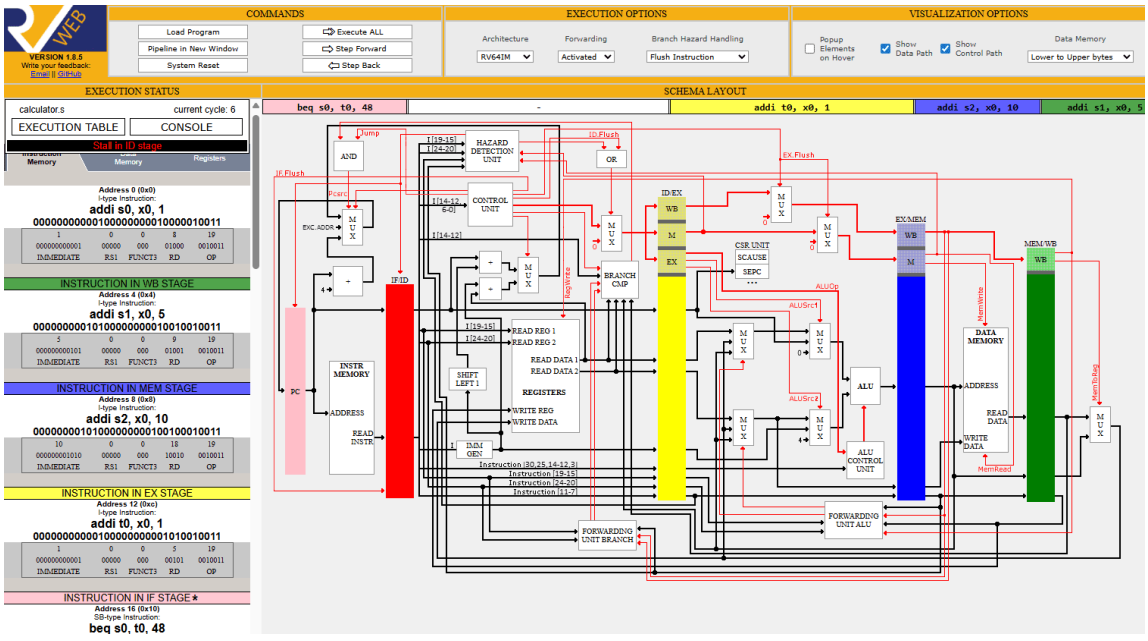

Figure 1. WebRISC-V main page.

3.2. Software Functionalities of WebRISC-V

- The visualization of the complete architectural schematic of a pipelined RISC-V (see Fig. 1);
- The ability of stepping forward and backwards in the execution of code, to better study what is happening inside the pipeline and its elements;
- On a single page view, the monitoring of the information about the current processing state (e.g., cycle count, colored tags to indicate the current stage of an instruction, highlighting of eventual 'bubbles' in the pipelined execution);
- A descriptive explanation of each internal element together with its current state, that can be shown by simply hovering with the mouse.
- The ability of simulating multiple hazard resolution modes of the pipeline;
- The possibility of enabling or disabling the data forwarding units (with automatic visualization of the corresponding schematic);
- The possibility of visualizing the memory segment contents (Text Segment, Static Data Segment, Dynamic Data Segment) and the registers.
- An online editor, with some built-in examples, and a contextually visible full list of the available instructions and directives.

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- Automatic generation of the classic pipeline diagram (see Fig. 2a); in case of loops, this diagram can be automatically squashed. (see Fig. 2b);
- Basic I/O system calls of the simulated RISC-V are possible by prompting the user via a popup window that emulates the system console.

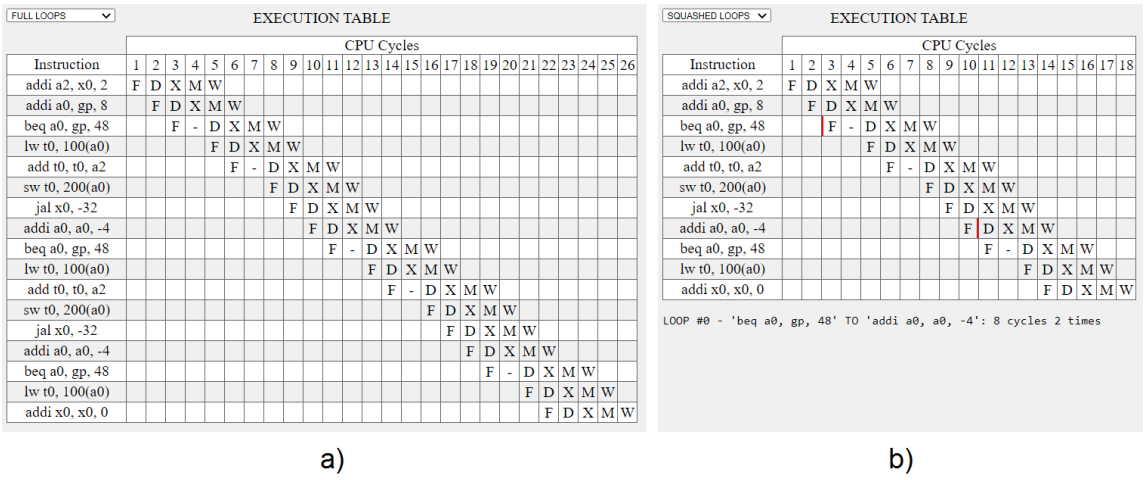

Figure 2. Pipeline diagram in both visualization methods: (a) 'Full loops' and (b) 'squashed loops'.

4. Use Cases in Education

WebRISC-V is designed for educational use, particularly in undergraduate computer architecture courses. Professors can use it to demonstrate pipeline execution principles, while students can experiment with different instruction sequences to observe their effects on performance. The tool aids in understanding the impact of forwarding, stalls, and branch hazards, making abstract concepts more tangible. Moreover, its web-based nature ensures accessibility without installation barriers, facilitating both classroom and remote learning. This paper is as a short introduction to WebRISC-V: more details can be found in[5].

4.1. GitHub Repository

The WebRISC-V source code and documentation are publicly available on GitHub: https://github.com/Mariotti94/WebRISC-V

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Statements and Declarations

Contribution Statement

RG is responsible for the complete writing of this paper, he was the supervisor of the MEng thesis which led to the realization of this tool and the designer of the UI of the tool. GM is the author and maintainer of the software that realized this tool.

Footnotes

[1] In a few words, a RISC-V 'module' is a subset of instructions.

References

1. ^*Petersen MB (2019). "Ripes." Morten Borup Petersen.*
2. ^*Nixon R (2012). Learning PHP, MySQL, JavaScript, and CSS: A Step-by-Step Guide to Creating Dynamic We bsites. O'Reilly Media, Inc. ISBN 9781449319267.*
3. ^*Waterman A, Asanovic K (2019). "The RISC-V Instruction Set Manual, Volume I: Unprivileged ISA." Andrew Waterman, Krste Asanovic.*
4. ^*Patterson DA, Hennessy JL (2017). Computer Organization and Design RISC-V Edition: The Hardware Soft ware Interface. 1st ed. San Francisco, CA, USA: Morgan Kaufmann Publishers Inc. ISBN 9780128122754.*
5. ^*Mariotti G, Giorgi R (2022). "WebRISC-v: A 32/64-bit RISC-v Pipeline Simulation Tool." ELSEVIER Softwar eX. **18**:1–7.*

Declarations

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