Research Article

WebRISC-V: A 64-bit RISC-V Pipeline Simulator for Computer Architecture Classes

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WebRISC-V is a web-based educational tool designed to simulate the pipelined execution of assembly programs according to the RV64IM specifications (64-bit RISC-V processor). The tool allows users to investigate pipeline stalls, understand the internal state of pipeline architectural blocks, and visualize the cycle-by-cycle execution of instructions. WebRISC-V executes directly in a web browser, providing a detailed pipeline execution for RISC-V processors. This paper describes the features of WebRISC-V, compares it with similar tools, and provides an example of its usage in investigating the pipeline.

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Introduction

Instruction pipelining is a fundamental concept in Computer Architecture courses, as it significantly improves processor performance. However, its real impact is often underestimated or misunderstood by students. WebRISC-V addresses this educational gap by offering an interactive, web-based tool that allows users to visualize and analyze pipeline execution in a user-friendly manner.

Understanding pipeline behavior, including stalls and hazards, is crucial in optimizing processor performance. WebRISC-V provides a cycle-by-cycle analysis of RISC-V instructions in a pipeline, allowing users to gain a deeper understanding of execution flow, instruction dependencies, and bottlenecks that affect speedup.

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Key Features and Contributions

WebRISC-V introduces several innovations that distinguish it from existing tools, including:

- A browser-based interface requiring no installation, making it accessible from any device.
- Cycle-accurate visualization of pipeline execution, via instruction flow and hazard detection.
- Identification and classification of stalls, hazards, and structural dependencies within the pipeline.
- Interactive features for modifying instructions and observing real-time execution changes.
- A side-by-side comparison of different execution sequences, providing insights into pipeline optimization.
- Automatic generation of detailed pipeline execution diagrams, aiding in teaching and research.
- A comparison with other available pipeline visualization tools, highlighting WebRISC-V's advantages in usability and accuracy.

Other Existing Pipeline Tools

Several tools exist for visualizing pipeline execution, but most require local installation and lack detailed cycle-by-cycle analysis. WebRISC-V stands out due to its web-based accessibility and real-time feedback. Tools such as Ripes and QtSPIM provide some pipeline visualization but do not offer the level of detail or interactivity as WebRISC-V. By allowing users to interact directly with the execution process, WebRISC-V serves as a more effective learning tool. PBSE, (MARS plug-in), MIPS X-Ray (MARS plug-in), DrMIPS, Mipster32, UCOMIPSIM, Visimips, WASP and WebMIPS are MIPS ISA tools; Ripes[1] and WebRISC-V are similar tools, but supporting the RISC-V ISA. While Ripes supports gcc-compiled code and is more tailored to developers, WebRISC-V restricts the supported ISA to 'RV64IM' to provide an environment more focused on educational principles.

Software Architecture

WebRISC-V has its back-end written in PHP and its front-end in HTML, CSS and JavaScript[2]. Being a server-side web application, it is installed and executed on a web server and presented to the user on their client interface. If the teaching staff wants a local installation, an instance can be hosted with a simple procedure on a Linux or Windows server.

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This simulator supports the full implementation of two RISC-V 'modules'[1] as they are described in the RISC-V ISA unprivileged specification[3]: the 64-bit Base Integer ("fence" instruction excluded) module - also called 'RV64I' module - and the Extension for Integer Multiplication and Division module - also called 'M' module, therefore making the tool run according to the 'RV64IM' specification.

Voluntarily, for easier student reference, WebRISC-V closely resembles the schematic used in the Patterson/Hennessy book[4], in which the pipelined datapath implementation is explored and explained.

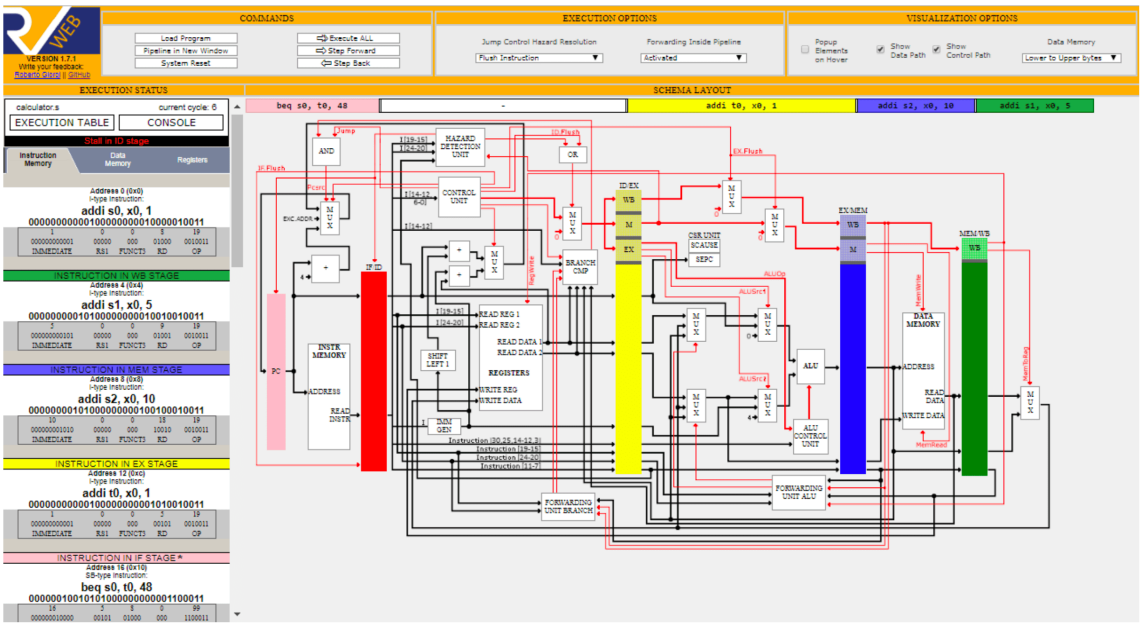

Figure 1. WebRISC-V main page.

Software Functionalities of WebRISC-V

- The visualization of the complete architectural schematic of a pipelined RISC-V (see Fig. 1).
- The ability to step forward and backward in the execution of code, to better study what is happening inside the pipeline and its elements.
- On a single page view, the monitoring of the information about the current processing state (e.g., cycle count, colored tags to indicate the current stage of an instruction, highlighting of eventual 'bubbles' in the pipelined execution).
- A descriptive explanation of each internal element together with its current state, that can be shown by simply hovering with the mouse.

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- Forwarding/No-Forwarding simulation modes.
- The possibility of enabling or disabling the data forwarding units (with automatic visualization of the corresponding schematic).
- The possibility of visualizing the memory segment contents (Text Segment, Static Data Segment, Dynamic Data Segment) and the registers.
- An online editor, with some built-in examples, and a contextually visible full list of the available instructions and directives.
- Automatic generation of the classic pipeline diagram (see Fig. 2a); in case of loops, this diagram can be automatically squashed (see Fig. 2b).
- Basic I/O system calls of the simulated RISC-V are possible by prompting the user via a popup window that emulates the system console.

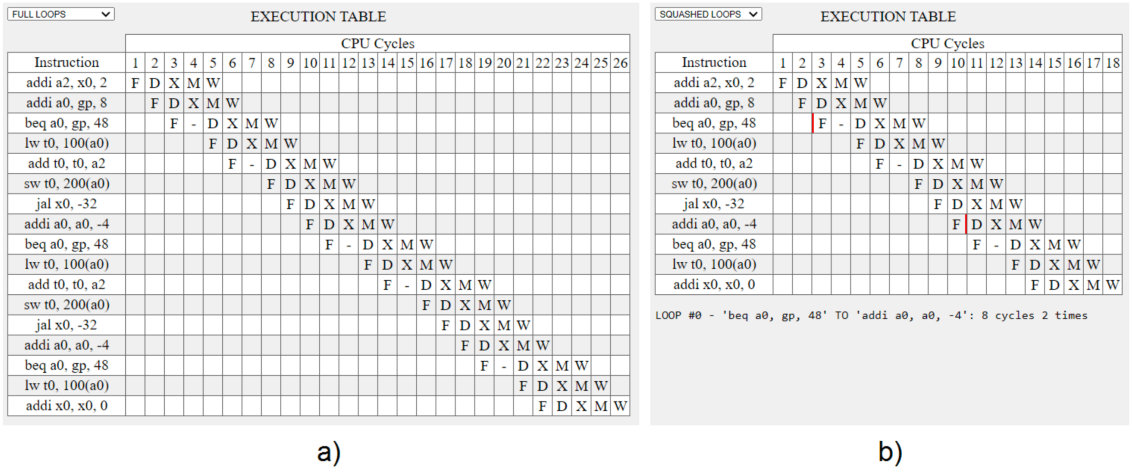

Figure 2. Pipeline diagram in both visualization methods: (a) 'Full loops' and (b) 'squashed loops'.

Use Cases in Education

WebRISC-V is designed for educational use, particularly in undergraduate computer architecture courses. Professors can use it to demonstrate pipeline execution principles, while students can experiment with different instruction sequences to observe their effects on performance. The tool aids in understanding the impact of forwarding, stalls, and branch hazards, making abstract concepts more tangible. Moreover, its web-based nature ensures accessibility without installation barriers, facilitating both classroom and remote learning [5].

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GitHub Repository

Source code and documentation are publicly available: https://github.com/Mariotti94/WebRISC-V

Footnotes

[1] In a few words, a RISC-V 'module' is a subset of instructions.

References

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4. ^*Patterson DA, Hennessy JL. Computer Organization and Design RISC-V Edition: The Hardware Software Interface. 1st ed. Morgan Kaufmann; 2017. ISBN 0128122757, 9780128122754.*
5. ^*Mariotti G, Giorgi R (2022). "WebRISC-V: A 32/64-bit RISC-V pipeline simulation tool". SoftwareX. 18: 1–7. doi:10.1016/j.softx.2022.101105.*

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