Review of: "Magnetic memory driven by topological insulators"

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Magnetic memories are data storage devices used in all manner of mainstream digital computing. While many types of devices (flash, memristors, phase-change materials, etc.) can implement memory cells, one of the most popular ones is a magnetic tunnel junction (MTJ) made of two ferromagnetic layers separated by an insulator. It is a non-volatile device with two resistance states - high and low - that can encode the binary bits 0 and 1 for binary logic or memory, much like the way a transistor's high and low resistance states encode the bits 0 and 1. The difference is that the MTJ is non-volatile and the bit encoded in the resistance state is preserved after power to the device is turned off, whereas a transistor is usually volatile and loses any memory of the encoded bit after it is powered off. On the flip side, the energy dissipated to switch a modern day transistor from one conductance state to the other is only about 100 aJ, whereas the energy dissipated to switch an MTJ by the commonly used method of spin transfer torque is about three orders of magnitude larger and the switching is also slower. Spin transfer torque (STT) requires passing a large spin-polarized charge current through the MTJ and that causes large energy dissipation, not to mention some damage to the MTJ. Spin-orbit torque (SOT) switching is a variation of STT where no charge current is passed through the MTJ, but a dissipationless spin current is passed through it by employing a phenomenon known as the giant spin Hall effect. The spin current is generated by passing a charge current through an adjacent material such as a heavy metal or a topological insulator. SOT has both advantages and disadvantages compared to STT. The advantages are that the energy dissipation can be reduced, and since no charge current passes through the MTJ, electromigration related damages within the MTJ are ameliorated. The major disadvantage is that SOT devices are 3-terminal because the read and write paths for passing the reading and writing currents are separate, while the STT device is 2-terminal and hence has a smaller footprint. In memory applications, the density (footprint) is often the primary consideration, which is why SOT memory has not yet replaced STT memory.

The efficiency of SOT switching depends on the amount of spin current generated for a given charge current, or in other words, the ratio of the two current densities which is called the spin Hall angle. This angle is usually very small, but it can be quite large (on the order of 0.1) when the charge current is passed through a heavy metal with strong spin-orbit interaction. However, there is an even better option, which is to replace the heavy metal with a topological insulator (TI) which is a material that is insulating in the bulk, but conducting in the surface. Furthermore, the current flowing along the surface of a TI is spin-polarized because of a phenomenon known as spin-momentum locking. So, if an MTJ is placed atop a topological insulator, a spin current will be injected into the MTJ which will switch it. The effective spin Hall angle of a TI can exceed unity. There is one small caveat however. Usually the magnetic layer of the MTJ that is in contact with the TI is metallic and it can shunt the current away from the surface of the TI which is more resistive than the magnetic layer. That would hinder switching. This problem can be mitigated by interposing a thin insulating layer between the MTJ and the TI.

Although it has been known for sometime that a TI is a better replacement for a heavy metal when it comes to SOT switching, the paper in question presents experimental verification of this edict. The paper has demonstrated low current density switching, which is certainly an encouraging start. Issues that still remain to be addressed are the actual energy dissipated to switch and how it compares with voltage controlled magnetic switching such as voltage controlled magnetic anisotropy or voltage controlled strain. The reported switching delay is well above 1 ns and that needs to be reduced without expending too much excess energy. Finally, it is important to estimate the switching error rate or write error probability since low energy switching usually tends to be error-prone.