Qeios

Peer Review

Review of: "DRC-Coder: Automated DRC Checker Code Generation Using LLM Autonomous Agent"

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1. Introduction

This paper proposes an AI framework that uses a generative language model to write DRC code, which is essential for semiconductor design. To this end, the DRC script-making process is broken down into interpretation and programming tasks to use two LLMs, and VLMs are incorporated herein to effectively process multimodal information, including text descriptions and layout representations.

2. Summarized characteristics & expected contribution

a. Summarized characteristics

(1) Innovation in automation: The proposed system is built on a multi-agent framework, which consists of two LLM agents that independently handle design rule interpretation and code generation, and an additional VLM component integrated to analyze visual elements and layout constraints.

(2) Automated Debugging and Verification: The system incorporates a built-in mechanism for debugging generated codes, significantly reducing human intervention and improving accuracy.

(3) High performance in accuracy and speed: The researchers tested the system on a set of standard cell layout rules, achieving a perfect F1 score of 1.000 in validation experiments. The generated DRC codes were produced within an average of four minutes, demonstrating efficiency and reliability.

b. Expected contribution

DRC is an essential rule for designing a chip considering process limitations, but it takes a considerable amount of time for an engineer to achieve proficiency in DRC, as pointed out in the paper, and it also takes a lot of time to set up the final DRC code by repeating the process of writing it, applying it to the designed chip layout, and testing it. In addition, since the number of patterns is large

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and complex due to continuous chip size reduction, even running DRC code once for a full-chip layout is rather time-demanding.

Therefore, the idea of this paper is timely and appropriate as it points out where AI should be used for EDA. It is expected that the method proposed by this paper will dramatically reduce the time to write the DRC code and also greatly help the engineers in charge to improve their understanding of the DRC.

3. Suggestions for improvement

a. VLM accuracy consideration: In the way VLM is combined and operated, it would be necessary to further check whether it will work well even for tiny and complex patterns while accurately recognizing their coordinates, such as the database unit (DBU).

b. Enhancement of code interpretability: It is also suggested to add explanatory comments or visualization tools for generated DRC codes.

c. Scalability to complex rules: The research does not extensively discuss the system's performance with highly complex or customized DRC rules. Future studies should explore scalability across different technology nodes.

4. Conclusion

In summary, the paper did great, pioneering work on the way of applying LLM to the EDA industry, with the appropriate problem definition and the approach to solving it. A follow-up paper is desired to verify that the method proposed by this paper works well for a wider variety of chip designs. I hope that this will eventually allow chipmakers to consider applying the method of this paper to actual chip design for mass production.

Declarations

Potential competing interests: No potential competing interests to declare.