Qeios

Peer Review

Review of: "WebRISC-V: A 64-bit RISC-V Pipeline Simulator for Computer Architecture Classes"

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The paper presents WebRISC-V, a 64-bit RISC-V Pipeline Simulator. The tool is intended to be used for educational purposes, helping students understand the details of the inner workings of a CPU system.

As a suggestion for improvement, I would suggest the possibility of having, in addition to the low-level view, a more high-level view that may represent higher-level concepts such as functions, in order to show function calls as bars, displaying the “function calls” in a timing visualization that could run in parallel to the view of the pipeline. In this way, the user would enable a “high-level view” where it would be possible to position on interesting function parts, and then by clicking “zoom” to the pipeline parts... A similar tool doing this kind of “visual positioning” is the traditional debugger that, from the instruction trace, allows positioning the view to the C/assembly code.

Declarations

Potential competing interests: No potential competing interests to declare.

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