Review of: "Fast Addition for Multiple Inputs with Applications for a Simple and Linear Fast Adder/Multiplier And Data Structures"

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Potential competing interests: No potential competing interests to declare.

The proposed method looks similar to ripple-carry adders to me. The main point of the paper is that the result of the ripple-carry adder does not change anymore, as soon as all carry bits are zero. The patent proposes to check all carry bits for zero after a full adder has finished and stop the calculation eventually. The work assumes that the check for zero of an n-bit vector happens with complexity O(1).

Actually, the work could be presented in a more direct way. In the paper, sum-bits are presented as a bit vector. The same holds for carry bits. A presentation based on the ripple-carry-adder would be much appreciated. The number of required steps of calculation is the length of the longest ripple-carry path, i.e. linear in the worst case.

After all, I wonder where precisely is the novelty in this work.