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Peer Review

Review of: "Negative Capacitance Effect at the Interface Between Si Wafers with Undulating Surfaces"

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In this manuscript, a novel structure is introduced that demonstrates negative capacitance behavior between two silicon wafers. Nevertheless, there are several aspects that require the authors to provide more comprehensive explanations and implement necessary revisions.

1. The dimensions of the proposed structure appear to be excessively large. The issue of scaling is critical for applications involving devices and integrated circuits, particularly as transistors utilizing ferroelectric materials are typically fabricated and characterized at the nanometer scale. The manuscript does not articulate the advantages of this method compared to previously established structures. Based on the figures presented, the challenges associated with fabricating this structure at reduced dimensions are evident, which raises concerns regarding compatibility with existing CMOS technology.

2. The manuscript lacks specification regarding the crystal orientation of the aluminum utilized on the silicon wafer. This parameter should be reported in conjunction with the work function employed.

3. The manuscript does not specify the distance (d) between the two silicon wafers, which is crucial since the tunneling current is significantly influenced by the separation between the electrodes.

4. It is essential to define any abbreviations, such as SEM, upon their first occurrence in the text.

5. The caption for Figure 3 requires further elaboration to enhance clarity.

6. The values presented in the second paragraph on page 4 and on page 5 should be verified for accuracy.

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Declarations

Potential competing interests: No potential competing interests to declare.