Review of: "Ge-Source Based L-Shaped Tunnel Field Effect Transistor for Low Power Switching Application"

Chan Shan[1]

1 Jimei University

Potential competing interests: The author(s) declared that no potential competing interests exist.

The authors propose a Ge-Source Based L-Shaped Tunnel Field Effect Transistor. Basically, this paper is interesting to the readers. However there are many comments and questions.

1、In the introduction part, the authors mention that some technical issues can be entangled by using different design approaches, and refer to relatively old papers [12]-[14]. This should of course be updated, such as the ones presented below:

a. Optimization of Hetero-Gate-Dielectric Tunnel FET for Label-Free Detection and Identification of Biomolecules, *IEEE Transactions on Electron Devices*, vol. 67, issue 5, pp 2157 - 2164, 2020.

b. In-Built N+ Pocket Electrically Doped Tunnel FET With Improved DC and Analog/RF Performance, *Micromachines*, vol. 11, issue 11, pp 960, 2020.

c. Characteristics of InAs/GaSb Line-Tunneling FETs With Buried Drain Technique, *IEEE Transactions on Electron Devices*, vol. 68, issue 4, pp 1537 - 1541, 2021.

2、The English grammar in the article should be carefully checked. For instance, in the Results and Discussion B. section, the sentence " It is evident from the results that the proposed LTFET works very efficiently from for. " is clearly not finished. The spelling and wording in the entire paper should be carefully checked.

3、SS is mentioned many times in the article, but the authors do not indicate whether it is average SS or point SS.

4、The authors say that F=average junction field in Eq. (1), however, I could not find F in Eq. (1).

5、In Fig.2, why is it the same Id-Vgs curve for Si source with and without pocket TFET?

6、Please explain how the Ion、Ioff, Vth and SS are calculate in Table 1.

7、The simulation results in Figure 3 do not match Figure 2. Please explain why.

8、In Optimization of Proposed Device A. part, the tunnelling model should be determined by the principle of the device, not by the best results of the simulation.

9、In Fig.5, why the curve of 1E18 is optimal, please explain it from the point of energy band.

10、The explanations of Fig. 6 and Fig. 7 are missing. Please explain it from the point of energy band.

11、In Fig.7, what is the logic behind choosing the metal work functions from 4.3 to 4.7. What are these metals? Are these metals being used in CMOS technology or the potential to be used in future CMOS

technology?

12Figure 10 is very blurry, and as can be seen from the energy band diagram, the mesh is too large, resulting in discontinuity of energy. Further, the authors should mark the length of the tunnelling path in the figure.

13Fig. 12 shows the influence of Vds variation on threshold voltage, transconductance (gm), and subthreshold swing (SS). I think there should be more parameters here, such as gm/Ids, drain output conductance, early voltage, intrinsic gain, cut-off frequency etc.