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Peer Review

Review of: "WebRISC-V: A 64-bit RISC-V Pipeline Simulator for Computer Architecture Classes"

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This work presents a RISC-V architecture simulator that exploits visual tracking of instructions in the pipeline. The simulator implements a basic RISC-V-based pipeline architecture, capable of simulating system calls to emulate functions such as `printf` in a console.

As a teaching tool, it is a good idea mainly because of the student's interaction with the simulator. Finding more interactive and visual solutions is always better for teaching complex topics such as computer architecture.

The simulator has interesting features, but it could be improved by adding more attractive, visual, and innovative elements, such as data transfer visualizations between modules and activation tracking of module and control flags per instruction.

As a research paper, the work could be improved, as the information provided in its current state is weak. Many simulators are mentioned without any references, and there is no evaluation of their features in comparison with other simulators. Features like usability, compatibility, instruction support, and visual level can be compared with other simulators to see the simulator's advantages.

Declarations

Potential competing interests: No potential competing interests to declare.

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