Qeios

Peer Review

Review of: "WebRISC-V: A 64-bit RISC-V Pipeline Simulator for Computer Architecture Classes"

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The article describes a tool that can be of great help to computer architecture teachers using RiscV. The paper is short and only describes the tool externally (no detail on the internal implementation other than the language used). It is a good article to present the tool to teachers/potential users, but it does not represent a real research contribution per se.

I would happily rate it as an “accept” or even a “strong accept” in a tool-paper track of an education-oriented conference, but I'm uncomfortable rating it in a more general context. Many traditional conferences/journals would reject it for not being a research paper, but I still think the paper deserves to be published somewhere.

I would have appreciated a discussion on the client-side vs. server-side architecture. Today's browsers are very capable, and doing a full client-side application, e.g., using WebAssembly, is clearly an option that could be considered, and it makes the server-side part straightforward to host. This is what https://riscv.vercel.app/ does, for example, and a comparison with this tool would be needed for the final version of this paper.

Details to improve the paper:

- What is the difference between “Forwarding/No-Forwarding simulation modes” and “The possibility of enabling or disabling the data forwarding units”?
- Figure 1 is hardly readable. Even zooming in a lot, we get anti-aliased, pixelized tiny fonts. It's probably hard to make it better within the Qeios format, but perhaps a link to a full-resolution image would help.

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Declarations

Potential competing interests: No potential competing interests to declare.